REMARKS

Reconsideration of the rejections set forth in the Office Action dated February 7, 2005, is respectfully requested. The Examiner has rejected claims 1-20, and Applicants have amended claims 1, 9, 13, 15, and 17. Accordingly, claims 1-20 remain pending in the application. No new matter has been added by these amendments as can be confirmed by the Examiner.

Applicants would like to thank the Examiner for the interview held on May 2, 2005 with the undersigned. During the interview, the undersigned attorney and the Examiner discussed the claims as well as the cited references: Rajski et al., United States Patent No. 6,327,687, (hereinafter "Rajski"); and Rohrbaugh et al., United States Patent No. 6,067,651 (hereinafter "Rohrbaugh").

A. Acceptance of Application Papers

Applicants note with appreciation the indication in the Office Action that the drawing sheets filed on May 8, 2001, have been deemed acceptable by the Examiner.

B. No Motivation Exists to Modify the Teachings of Rajski or Rohrbaugh such that the Patentability of Amended Claims 1-20 is Precluded Under 35 U.S.C. § 103(a)

The Examiner rejected claims 1-20 under 35 U.S.C. § 103(a) as allegedly being rendered obvious by Rajski in view of Rohrbaugh.

First, in the Office Action, the Examiner alleges that claims 1-20 do not recite that the test vectors are targeted at a "plurality of faults" prior to filling any of the non-care bits of the original test vector with repeated values in the manner set forth in more detail in the prior Amendment, dated December 16, 2004. Without acquiescing, Applicants have amended claims 1, 9, 13, 15, and 17 to more clearly set forth the chronology of claim elements by which the claimed system and method reduces test data volume. Claims 1, 9, 13, 15, and 17 therefore have been amended to more

explicitly recite that the test vectors are targeted at a "plurality of faults" ***prior to*** filling any of the non-care bits of the original test vector with repeated values. As discussed in the prior Amendment, this feature is supported throughout the specification, with exemplary citations found at page 1, lines 13-15 and page 4, lines 2-9.

Applicants respectfully submit that this feature is an important distinction between Rohrbaugh and Rajski, as it is totally missing from Rajski and Rohrbaugh. With reference to amended claim 1, for example, Rajski and Rohrbaugh fail to disclose or suggest generating original test vector data that *targets a plurality of faults* and includes care bits and non-care bits **and thereafter filling the non-care bits with a repeated value** to form a compressible test vector data set. For example, Rohrbaugh teaches:

> *In contrast, dynamic compaction operates to generate compacted vectors one at a time. More specifically, a first test vector is generated to test for a given fault in a list of faults to be tested (just like the first test vector generated in static compaction).* However, before generating a second test vector, an attempt is made to utilize the first test vector to test for additional faults. In this regard, the unused bit positions (i.e., don't care values) may be set to either "1"s or "0"s, or existing bit positions may be utilized, to the extent that the values need not be changed.
>
> Rohrbaugh, Col. 2, lines 53-62 (italics added).

Thus, as can be seen, Rohrbaugh teaches that a test vector is generated for a fault. After this vector is created, Rohrbaugh compresses the vector for this first fault before generating a new test vector for the next fault that must be tested. Once this next test vector is created, this next test vector is compressed.

In contrast to Rohrbaugh, the presently claimed invention creates vectors targeting "a plurality of faults" and then, once those vectors targeted at the plurality of

faults are created, compresses the plurality of test vectors. This is totally different than both Rajski and Rohrbaugh.1

Accordingly, Rajski and Rohrbaugh do not render amended claims 1, 9, 13, 15, and 17 obvious; therefore, claims 1-20 are in condition for allowance.

C. Rajski and Rohrbaugh Also Fail to Teach or Suggest the Further Claim Elements Recited in the Dependent Claims such that Patentability is Precluded

In addition to the reasons set forth above with reference to the amended independent claims 1, 9, 13, 15, and 17, Applicants respectfully submits further grounds to support that the dependent claims 2-8, 10-12, 14, 16, and 18-20 are not rendered obvious by Rajski and Rohrbaugh and are in condition for allowance.

On pages 9-10 of the Office Action dated January 30, 2004 and referenced by the pending February 7, 2005, Office Action, the Examiner discusses the patentability of dependent claims 2-8, 10-12, 14, 16, and 18-20 in light of Rajski. With reference to the rejection of claim 2, for example, the Examiner asserts that "Rajski teaches (col. 4, lines 55-68) transmitting the compressed test data to a test system and acquiring the compressed [sic, "decompressed"] care bits for testing the integrated circuit." See January 30, 2004, Office Action at p. 9, ll. 3-4.

In actuality, the referenced passage in Rajski discloses:

> A method according to the invention is used to generate a compressed test pattern to be applied to scan chains in an integrated circuit under test. **The compressed test pattern is stored in an ATE and is applied on input channels to an integrated circuit being tested.** A clock signal is used to synchronize transfer of data (the compressed pattern) from the ATE to the integrated circuit. **The compressed pattern is**

1 Note that Rohrbaugh does check to see if the vector created for the first fault will also work for additional faults. This check, however, is not the same thing as actually creating test vector data "targeted" to a plurality of faults. In effect, Rohrbaugh checks to see if by chance the vector data created for the first fault is applicable to additional faults, while the presently claimed invention creates data "targeted" to a plurality of faults.

> **decompressed on the integrated circuit** to obtain a test pattern, which is passed to scan chains to test faults within the integrated circuit. The scan chains include a plurality of scan cells (memory elements) coupled together that store the test pattern.
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> Rajski, col. 4, ll. 55-68 (emphasis added).

In contrast to Rajski, the method of dependent claim 2 recites the step of "recovering the care bits of said original test vector data from said compressed vector data set, for loading into input latches of a tester in said test system." **The method of claim 2 therefore inverts the teaching of Rajski.** Rather than applying compressed data to the device under test and recovering the original data within the device under test, claim 2 sets forth that the original data is recovered prior to being loaded into the input latches. Accordingly, it is submitted that Rajski does not preclude the patentability of claim 2 and that claim 2 is in condition for allowance.

Turning to the rejection of claims 3 and 18, the Examiner contends that Rajski "teaches generating a background vector data set (generate a test cube, 62) in Figure 5" and "teaches forming a differential vector data set by XORing care bits with background vector bits in Fig. 7." See January 30, 2004, Office Action at p. 9, ll. 5-7. In discussing the test cube 62 with reference to Fig. 5, Rajski states that:

> In process block 62 (FIG. 5), a test cube is generated. **The test cube is a deterministic pattern of bits wherein each bit corresponds to a scan cell in the scan chains. Some of the scan cells are assigned values (e.g., a logic 1 or logic 0), while other scan cells are "don't cares."** The scan cells that are assigned values are used in the compression analysis and are represented in the compressed test pattern. The remaining scan cells that are "don't cares" need not be represented in the compressed test pattern and are filled with a pseudo-random values generated by the decompressor.
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> Rajski, col. 8, ll. 51-61 (emphasis added).

Claims 3 and 18 recite the generation and use of a background vector data set, which is defined as being either "all 0s, all 1s, or a random distribution of 0s and 1s."

See page 5, ll. 1-2. Instead of disclosing the generation or use of such a background vector data set, Rajski teaches the generation of a test cube in which "[s]ome of the scan cells are assigned values (e.g., a logic 1 or logic 0), while other scan cells are "don't cares." **Rajski therefore neither discloses or suggests the generation or use of a background vector data set in the manner set forth in claims 3 and 18.** Therefore, Applicants submit that claims 3 and 18 are in condition for allowance.

Claim 5 recites a step of "attaching a header to said differential vector data set, said header identifying an algorithm and seed used to generate said background vector data set." In rejecting claim 5, the Examiner argued that Rajski "teaches an algorithm (Gauss-Jordan elimination) used in header identification and a seed used to generate vector data in column 10, line 65 through column 11, line 20: 'Gauss-Jordan techniques ... It can be verified ... resulting seed variables.'" See January 30, 2004, Office Action at p. 9, ll. 10-13. The Examiner relies on the following passage from Rajski to support the rejection of claim 5:

> [A] corresponding compressed test pattern can be determined by solving the following system of ten equations from FIG. 7 using any of a number of well-known techniques such as Gauss-Jordan elimination techniques. The selected equations correspond to the deterministically specified bits... It can be verified that the resulting seed variables a_0, a_1, a_2, a_3 and a_{13} are equal to the value of one while the remaining variables assume the value of zero. This seed will subsequently produce a fully specified test pattern in the following form...
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> Rajski, col. 10, ll. 62-67; col. 11, ll. 1-20 (Table 3 omitted).

In contrast to the argument of the Examiner, **Rajski does not discuss the use of headers** in the cited passage, much less teach the step of "attaching a header to said differential vector data set." Accordingly, Applicants submit that Rajski does not preclude the patentability of claim 5 and that claim 5 is in condition for allowance.

The Examiner likewise rejected dependent claims 6, 8, and 19 based upon Rajski. Turning to the rejections of claim 6, the Examiner alleged that Rajski teaches "decompressing the compressed test vector data (decompressor, 36) in Figure 2" "extracting and reconstructing vector data in Figure 4," and "XORing the reconstructed background vector data to form a reconstructed test vector data in Figure 7." See January 30, 2004, Office Action at p. 9, ll. 14-17. The Examiner rejected claims 8 and 19 by asserting that Rajski "teaches a random distribution of bits having both '0' and '1' in column 3,lines 10-100: 'Weighted random patters have been primarily used.'" See January 30, 2004, Office Action at p. 9, ll. 20-21.

Claim 6 however **recites** the steps of "reconstructing said **background vector data set** from said header" and "XORing said reconstructed **background vector data set** with said extracted differential vector data set to form a reconstructed test vector data set." Whereas, **a background vector data set** that "comprises a random distribution of bits having values of both '0' and '1'" **is set forth in claims 8 and 19.**

As discussed above with reference to claims 3 and 18, **Rajski neither discloses or suggests the generation or use of a background vector data set**. Rajski therefore cannot, and does not, teach either "reconstructing said background vector data set from said header" or "XORing said reconstructed background vector data set with said extracted differential vector data set to form a reconstructed test vector data set" as alleged by the Examiner with reference to claim 6. Likewise, Rajski cannot, and does not, teach a background vector data set that "comprises a random distribution of bits having values of both '0' and '1'" as set forth in claims 8 and 19. Accordingly, Applicants submit that claims 6, 8, and 19 are in condition for allowance.

Accordingly, for at least the reasons set forth above, it is submitted that claims 1-20, as amended, are in condition for allowance. A Notice of Allowance is earnestly

solicited. The Examiner is encouraged to contact the undersigned at (650) 614-7660 if there is any way to expedite the prosecution of the present application.

Respectfully submitted,

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